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SEP 27 2002
PATENT & TRADEMARK OFFICE

Input/Output Subsystem

Fig. 6 EXAMPLE PERIPHERAL CONTROLLER BLOCK DIAGRAM

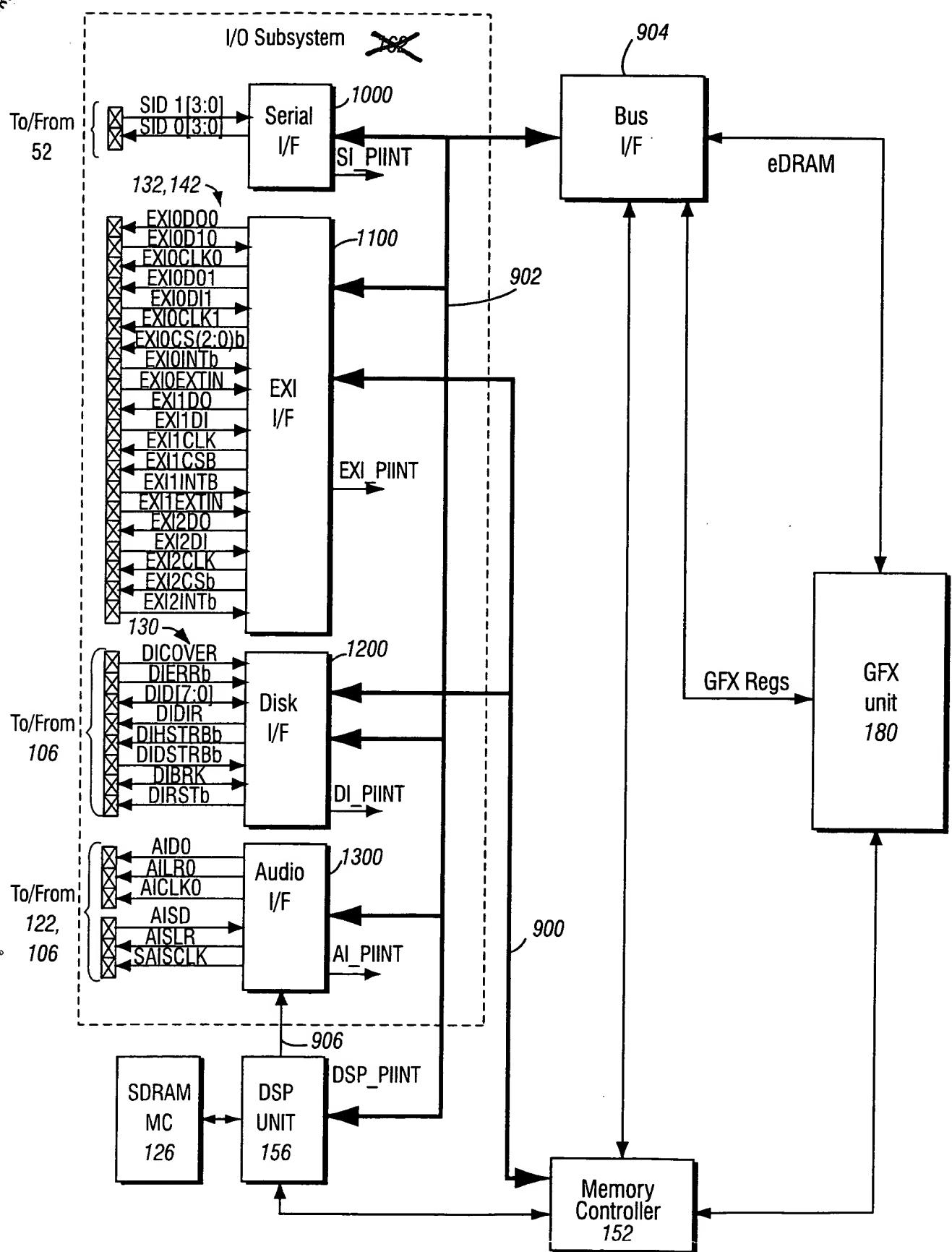


Fig. 3

